PTO/SB/05 (2/98)

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JC572 U.S. PTO 06/05/98

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	TI-25277
First Named Inventor or Application Identifier	Maureen A. Hanratty
Title	Antireflective Structure And Method
Express Mail Label No	EL071334925US

On Page 1 of the specification, before line 1, insert –This application claims priority under 35 USC § 119(e)(1) of provisional application number **60/049,006** filed **06/09/97**.--

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] *Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification *[Total Pages 12]* *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Bnef Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Descnption
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC d113)* *[Total Sheets 6]*
4. Oath or Declaration *[Total Pages 2]*
   - a. [X] Newly Executed (original or copy) **(UNSIGNED)**
   - b. [ ] Copy from a pnor application (37 CFR §1 63(d)) *(for continuation/divisional with Box 17 completed)*

   [Note Box 5 below]

   - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the pnor application, see 37 CFR §1 63(d)(2) and 1 33(b)
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identical of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & Documents(s))
9. [ ] 37 CFR §3 73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [ ] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *if foreign priority is claimed)*
16. [ ] Other

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information below and in a preliminary amendment:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: / .

Prior application information: ***Examiner*** _____ ***Group / Art Unit:*** _____

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

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Name (Print/Type)	W. James Brady	Registration No. (Attorney/Agent)	32,080
Signature	W James Brady	Date	06/05/98

Burden Hour Statement: This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12

TOTAL AMOUNT OF PAYMENT	($) 790

Complete If Known

Application Number	
Filing Date	06/05/98
First Named Inventor	Maureen A. Hanratty
Examiner Name	
Group / Art Unit	
Attorney Docket No.	TI-25277

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge to the following Deposit Account,

Deposit Account Number: **20-0668**

Deposit Account Name: **Texas Instruments Incorporated**

☒ Charge any additional fee required or credit any overpayment

☐ Charge all indicated fees and any additional fee required or credit any overpayment

2. ☐ **Payment Enclosed:**

☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	$790
106	330	206	165	Design filing fee	$
107	540	207	270	Plant filing fee	$
108	790	208	395	Reissue filing fee	$
114	150	214	75	Provisional filing fee	$

SUBTOTAL (1) ($)790

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	4	-20**=	0	x	$22	=	$0
Independent Claims	2	-3** =	0	x	$82	=	$0
Multiple Dependent					$270	=	$0

**or number previously paid, if greater; For Reissue, see below

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent Claims in excess of 3
104	270	204	135	Multiple dependent claims in excess of 3
109	82	209	41	**Reissue independent claims over original patent
110	22	210	11	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $790

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension of time within second month	
117	950	217	475	Extension of time within third month	
118	1,510	218	755	Extension of time within fourth month	
128	2,060	228	1,030	Extension of time within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a pubic use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (time number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1 129(b))	

Other fee (specify) _____

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	W. James Brady			Reg Number	32,080
Signature	W James Brady	Date	06/05/98	Deposit Account User ID	20-0668

ANTIREFLECTIVE STRUCTURE AND METHOD

RELATED APPLICATIONS

The following patent applications disclose related subject matter: Serial Nos. 08/678,847, filed 07/12/96 (TI-20565). These applications have a common assignee with the present application.

BACKGROUND OF THE INVENTION

The invention relates to electronic semiconductor devices, and, more particularly, to antireflective structures and fabrication methods for such structures.

Semiconductor integrated circuits with high device density require minimal size structures such as short gates for field effect transistors, small area emitters for bipolar transistors, and narrow interconnects between devices. The formation of such polysilicon or metal (or a stack of metals or a metal silicide on polysilicon) structures typically involves definition of the locations of such structures in a layer of photoresist on a layer of polysilicon or metal by exposure of the photoresist with radiation passing through a reticle containing the desired structure pattern. During the exposure, radiation reflected from the underlying material (e.g., polysilicon, metal, ...) can degrade the pattern developed in the photoresist, so include an antireflective coating or layer on the polysilicon or metal. Commercial antireflective coatings include organic materials and TiN which strongly absorb at the radiation wavelength, such as polymers with dye-groups for absorption.

After exposure and development of the photoresist, the underlying layers of antireflective coating plus material (polysilicon, metal, ...) are anisotropically etched using the patterned photoresist as the etch mask (or the antireflective coating may first be wet developed and then the underlying material anisotropically etched). Thus the minimal structural linewidth equals the minimal linewidth that can be developed in the photoresist.

One approach to overcome the linewidth limitation patterns photoresist and then isotropically etches the patterned photoresist to shrink its size and thereby emulate a

smaller original linewidth. However, this approach has a problem of the isotropic etch of the patterned photoresist also etches the antireflective coating.

Ogawa et al, 2197 Proc. SPIE 722 (1994) describes the use of silicon oxynitride as an antireflective coating on a oxide coated tungsten silicide layer and on an aluminum layer for i-line and deep ultraviolet radiation by quarter-wavelength thickness for reflective interference.

SUMMARY OF THE INVENTION

The present invention provides integrated circuit fabrication with a silicon oxynitride antireflective layer for gate location plus patterned photoresist linewidth reduction for gate length definition followed by interconnect definition without patterned photoresist linewidth reduction.

This has the advantages of an antireflective layer compatible with linewidth reduction and polysilicon etching.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings are heuristic for clarity.

Figures 1a-m are cross sectional elevation views of a preferred embodiment integrated circuit fabrication method steps.

Figure 2 illustrates the optical constant variation with composition.

Figure 3 shows net reflection.

Figure 4 illustrates linewidth reduction.

Figures 5a-d are cross sectional elevation views of another preferred embodiment.

Figure 6 shows a damascene preferred embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Overview

The preferred embodiments use a silicon oxynitride ($Si_xO_yN_z$) as an antireflective layer for patterning of photoresist on polysilicon followed by an isotropic etching of the patterned photoresist to reduce linewidth and then an anisotropic etcing of the oxynitride plus polysilicon to form gates and gate level interconnects; and lastly, overlying metal interconnects are formed using patterned photoresist without linewidth reduction but using a differing composition silicon oxynitride as antireflective layer due to the differing underlying material reflectivity.

The index of refraction and the extinction coefficient (real and imaginary parts of the square root of the dielectric constant) of silicon oxynitride vary with the composition (see Figure 2). Thus, essentially select the composition to have optical constants that adjust the reflected waves amplitudes according to the underlying material reflectivity and select the oxynitride layer thickness to provide quarter-wave interference so the reflected waves cancel.

The resultant integrated circuit may include residual silicon oxynitride on the gates or interconnects or both or neither.

First preferred embodiment

Figures 1a-m illustrate in cross sectional elevation views the steps of a first preferred embodiment fabrication methods for integrated circuits including field effect transistors (e.g., CMOS or BiCMOS). The example is of lithography which has 0.25 μm minimal linewidth and a circuit with 0.25 μm minimal metal interconnect width together with 0.18 μm minimal (silicided) polysilicon linewidth (gate length). The preferred embodiment includes the following steps:

(1) Start with a silicon (or silicon on insulator) wafer 102 with LOCOS or shallow trench isolation and twin wells for CMOS devices (optionally, plus memory cell array wells and bipolar device buried layers). Perform threshold adjustment implants (which may differ for cell transistors and various peripheral transistors), and form gate

dielectric. Deposit layer 104 of polysilicon gate material of thickness 300 nm; see Figure 1a.

(2) Deposit a 29 nm thick conformal layer 110 of (hydrogenated) silicon oxynitride by PECVD from a flow of silane and nitrous oxide; see Figure 1b. The composition of the oxynitride and thickness are selected according to the reflectivity of the underlying material; in particular, for polysilicon 104 take the composition to have a ratio of silicon to oxygen to nitrogen equal 53 to 38 to 9; the oxynitride also contains roughly 10% bound hydrogen, but the exact hydrogen fraction is difficult to measure. This composition gives measured optical constants of n = 2.11 and k = 0.55 (theoretical n = 2.15 and k = 0.60) and thus a layer thickness of 29 nm provides a quarter wavelength at 248 nm. See the following section on oxynitride composition.

(3) Spin on 900 nm average thickness layer 112 of photoresist which is sensitive to 248 nm radiation (deep ultraviolet); see Figure 1c.

(4) Expose photoresist 112 with 248 nm wavelength radiation through a reticle for gates and gate level interconnects; the exposed minimal linewidth may be about 250 nm. Silicon oxynitride 110 acts as an interference antireflective layer during exposure of photoresist 112. Develop photoresist 112; see Figure 1d which shows the differing heights of the patterned photoresist possible with LOCOS isolation.

(5) Shrink the patterned photoresist (reduce linewidth) with an isotropic etch which may be an oxygen-nitrogen plasma in a high density plasma reactor with small bias to limit ion bombardment for isotropy. The final minimal linewidth is 180 nm (although reduction to 60 nm may be achieved with good linewidth control). Thus the minimal linewidth photoresist shrinks from a 900 nm by 250 nm to roughly 850 nm by 180 nm; see Figures 1d-e.which shows (exaggerated) original patterned photoresist line 114 reduced to photoresist line 116.

(6) Remove the exposed portion of silicon oxynitride 110 with an anisotropic plasma etch using CF_4 or some other fluorine source; this etch also acts as the breakthrough etch (to eliminate surface oxides) for polysilicon 104 in the next step and may be performed immediately before and in the same chamber as the polysilicon etch. This etch also reduces the photoresist height to very roughly 700 nm; see Figure 1f.

(7) Use the remaining silicon oxynitride 110 plus photoresist as an etch mask for the anisotropic plasma etch of polysilicon 104 to form gates 106 and gate level interconnects 108. The etch may be a HBr plus oxygen plasma which is very selective to oxide and oxynitride. Thus even if the polysilicon etch strips the photoresist, the oxynitride antireflective layer remains and provides sufficient etch masking because of the etch selectivity. Figure 1g shows oxynitride-topped gates 106 plus gate level interconnects 108. The gate material could also provide a polysilicon emitter for bipolar devices which would require a prior base implant. Gates 106 are 300 nm high and 180 nm long (Figure 1g is a cross section along the gate length, and gates typically have widths much greater than their lengths).

(8) Perform lightly doped drain implants with the gate, oxynitride, and any residual resist as the implant mask; this also requires non-critical photolithographic masking for CMOS or BiCMOS circuitry which will also remove any residual resist. See Figure 1h.

(9) Form sidewall dielectric spacers 120 on the gates (and gate level interconnects) by conformal deposition of a dielectric layer followed by anisotropic etching. The sidewall dielectric may be silicon nitride and the anisotropic etch a plasma of fluorine plus an inert gas. This sidewall spacer etch will also remove some (or all) of the oxynitride on the tops of the gates and gate level interconnects. Introduce dopants to form sources and drains; see Figure 1i. A variation would be a self-aligned silicidation to create a silicide on both the gate top and the source/drains. This silicidation may be by stripping any remaining oxynitride from the gate tops and oxide from the source/drain surfaces, blanket metal (Ti or Co or Ni) deposition followed by reaction with underlying silicon, and then removal of unreacted metal (or TiN for the case of Ti silicidation in an nitrogen atmosphere). Figure 1j shows the resulting silicide.

(10) Form a planarized premetal dielectric layer 130 (such as reflowed BPSG or a stack of conformal and planarized layers, and the planarization may be by chemical mechanical polishing (CMP) or resist etch back). Then photolithographically define and etch vias through dielectric layer 120 for contact to the source/drains and the gate/interconnects; see Figure 1j. The antireflective layer for this lithography may also

be silicon oxynitride, but the transparency of underlying oxide makes the deeper reflections significant.

(11) For a structure with an embedded memory cell array using one-transistor one-capacitor memory cells, the bitlines and cell capacitors may be formed next. For clarity such steps are not illustrated and attendant additional dielectric layers deposited on dielectric 130 will just be considered part of dielectric 130 in the Figures.

(12). Blanket deposit (including filling vias) a metal stack such as 50 nm of Ti, 50 nm of TiN, 300 nm of W or Al (doped with Cu and Si), and 50 nm of TiN; the bottom Ti and TiN form a diffusion barrier and the top TiN forms an antireflective coating for lithography. Prior to the W or Al deposition the bottom Ti may be reacted with the source/drain to form a silicide to stabilize the metal-to-silicon contact. The Ti and TiN may be deposited by physical vapor deposition (PVD) or chemical vapor deposition (CVD) (e.g., TiCl4 + NH3 --> TiN + HCl); the aluminum may be deposited by PCD and then forced into the vias under high pressure or by CVD; and W may be deposited by CVD. Alternatively the vias may be filled with W by a CVD blanket deposition followed by an etchback to leave W only in the vias, and then an Al blanket deposition.

(13) Apply silicon oxynitride antireflection layer 150 on blanket metal 140; see Figure 1k. Again, select the oxynitride composition to give optical constants according to the reflectivity of the metal and take the oxynitride layer thickness to yield a quarter-wavelength. For example, with underlying aluminum and deep ultraviolet (248 nm) exposure, take n = 2.16 and k = 0.83; this implies a thickness of 248nm/4*2.16 = 29 nm. Note that the extinction coefficient is much larger than that of the oxynitride for the polysilicon; this is due to the greater reflectivity of the aluminum.

(14) Spin on photoresist and pattern it to define the first level metal interconnects; see Figure 1l with patterned resist 152 illustrating minimal linewidth of 250 nm. Again, a brief fluorine based plasma etch strips the exposed oxynitride without removing much patterned resist. Because the interconnects are wider than the gates, no resist linewidth reduction is needed.

(15) Use the patterned resist and oxynitride as the etch mask to anisotropically plasma etch the metal and thereby form interconnects 142; chlorine-based plasmas

with some fluorine for copper-doped aluminum and TiN, and fluorine-based plasmas for tungsten.

(16) Deposit a 50 nm thick conformal oxide liner 150 on interconnects 142 by plasma-enhanced decomposition of TEOS with oxygen or ozone. Liner 150 passivates the metal surfaces and prevents diffusion of metal atoms into the intermetal level dielectric, which may be a low dielectric constant material such as porous silica or fluorinated parylene. Then deposit the intermetal level dielectric over the liner-coated interconnects; the intermetal level dielectric may be a stack of two or more materials, such as porous silica between the first level interconnects and fluorinated silicon dioxide over the porous silica and interconnects.

(17) Form vias in the intermetal level dielectric analogous to the via formation of step (10). Then form second level interconnects on this intermetal level dielectric by a repetition of the foregoing steps (12)-(16). Similar repetitions may be used to form third, fourth, fifth, ... level interconnects.

Silicon oxynitride composition

Silicon oxynitride has an index of refraction and extinction coefficient depending upon composition as illustrated in Figure 2 with increasing nitrogen content increasing n and k. Thus silicon oxynitride as an antireflective layer provides two parameters (layer thickness and composition) to adapt to the underlying material reflectivity to yield a net zero reflectivity from the antireflectivity layer. In particular, consider the simplified situation of single reflections: radiation of intensity 1 passing through the photoresist impinges on the antireflective layer and a fraction r (typically about 5-10%) reflects (with a phase shift of π) back into the photoresist and 1-r passes through the antireflective layer with attenuation by a factor e^{-kt} where k is the extinction coefficient and t is the thickness of the antireflective layer. At the interface with the underlying material, a fraction R reflects (plus phase shifts by π) and the remainder transmits through and/or absorbs in the underlying material. The reflected fraction R is also attenuated by e^{-kt} as it passes back through the antireflective layer and reenters the photoresist. Thus the portion reflected from the underlying material is $R(1-r)e^{-2kt}$ and this is to cancel the

initially reflected portion r. To cancel, the amplitudes must equal ($r = R(1-r)e^{-2kt}$) and the phases must differ by π which implies the thickness t must be a quarter wavelength. The wavelength in antireflective layer is the radiation's in vacuo wavelength λ divided by the index of refraction n of the antireflective layer. Thus take $t = \lambda/4n$, and select the composition of the oxynitride to have the ratio k/n satisfying:

$$r = R(1-r)e^{-k\lambda/4n}$$

$$k/n = 4/\lambda\ [\log(R) + \log((1-r)/r)]$$

Of course, the reflectivity r depends upon n and k and the optical constants of the photoresist, but is relatively constant over a range n and k. Similarly, once the underlying material is known, R is approximately known (it also depends upon n and k), and the composition to give the desired k/n can be selected.

Figure 3 shows the computed net reflection back into resist as a function of the optical constants of the oxynitride with more precise modeling of reflections at the interfaces of resist-oxynitride and oxynitride-polysilicon for an oxynitride layer thickness of 29 nm. Inside the central contour shows the less than 1% net reflection into the resist. Also, Figure 3 shows the n-k relation curve of silicon oxynitride as in Figure 2 superimposed on the computed net reflections; the curve passes through the center of the region of less than 1% net reflection which indicates that targeting the composition at the center will give robust oxynitride parameters

Linewidth reduction

Figure 4 shows the robustness of the patterned resist linewidth reduction using oxynitride antireflective layer with a fixed oxygen resist etch (which removes 80 nm of resist) for various initial resist linewidths. Figure 4 indicates the standard deviation observed in the reduced linewidth by the three sigma curves in Figure 4. Thus a reduction from 220 nm to 60 nm has a standard deviation of roughly 2-3 nm. This robust large linewidth reduction using the silicon oxynitride antireflective layer permits

the original resist linewidth to be patterned in a range where the lithography is well controlled.

Disposable gate preferred embodiment

Figures 5a-d illustrate a disposable gate method of integrated circuit fabrication which uses the silicon oxynitride antireflective layer. In particular, follow the foregoing steps (1)-(9) to have a polysilicon dummy gate with sidewall spacers and source/drains formed in the substrate. Use the patterned resist reduction to make the dummy gate length only 60 nm; this can be achieved by an original dummy gate length of 220 nm followed by 80 nm resist etch (see Figure 4). The resulting structure is analogous to that of Figure 1i.

Deposit 500 nm thick dielectric, such as TEOS oxide, and planarize, such as by CMP, to expose the top of the polysilicon dummy gate. Figure 5a shows dummy gate 505 and dielectric 530; dummy gate 505 may be about 200 nm high and 60 nm long.

Etch out dummy gate 505 with an HBr + O2 plasma. Optionally, strip the gate oxide and thermally grow a new gate oxide at the bottom of the groove left by the removal of dummy gate 505. Next, blanket deposit gate material, such as TiN or a stack of different metals, to fill the groove plus cover dielectric 530; see Figure 5b showing 200 nm thick metal gate material 507.

Deposited 29 nm thick silicon oxynitride with composition (optical constants) adapted to the gate material, followed by spin on of photoresist sensitive to 248 nm radiation. Pattern the photoresist to define a gate top of length 250 nm, and use the patterned photoresist (without linewidth reduction) to etch gate material 507 to form T-shaped gate 506; see Figure 5c.

Continue as in foregoing step (10)-(17) by dielectric deposition, via formation, first level metal interconnect formation, and so forth. See Figure 5d.

Damascene preferred embodiment

The metal interconnect structure of the foregoing preferred embodiments can be replaced with a damascene interconnect structure because the photoresist linewidth

reduction is only used in the gate level. In particular, repeat the foregoing steps (1)-(12) with the variation in step (12) of first fill the vias, then deposit a second dielectric level, photolithographically define locations for grooves in the dielectric, next etch the dielectric to form the grooves, and then blanket metal with CMP or etchback to leave metal only in the grooves and thereby form the interconnects. Figure 6 illustrates the damascene structure for one metal level with gate 606, premetal level dielectric 630, filled via 644, and first metal level dielectric 650.

Modifications

The preferred embodiments can be modified in various ways while retaining the features of silicon oxynitride antireflective layer for resist linewidth reduction and linewidth reduction for gates together with no linewidth reduction for interconnects.

For example, the photoresist may be exposed at different radiation wavelengths, such as 193 nm, with corresponding adjustment in antireflective layer thickness.

CLAIMS

What is claimed is:

1. A method of fabrication of an integrated circuit, comprising the steps of:

(a) patterning a first layer of resist on a layer of gate material to define gate locations;

(b) reducing the linewidth of said patterned layer of resist of step (a);

(c) using said reduced linewidth patterned resist as an etch mask to form gates from said layer of gate material;

(d) forming a layer of dielectric on said gates;

(e) patterning a second layer of photoresist to define interconnects;

(f) using said patterned photoresist without linewidth reduction to form interconnects over said gates.

2. The method of claim 1, wherein:

(a) said using of step (f) of claim 1 is using the patterned photoresist as an etch mask for an underlying layer of metal.

3. The method of claim 1, wherein:

(a) said using of step (f) of claim 1 is using the patterned photoresist as an etch mask to etch grooves in underlying dielectric to be filled with metal.

4. A method of fabrication of an integrated circuit gate, comprising the steps of:

(a) patterning a first layer of resist on an antireflective layer on a layer of dummy gate material to define gate locations;

(b) reducing the linewidth of said patterned layer of resist of step (a);

(c) using said reduced linewidth patterned resist as an etch mask to form dummy gates from said layer of dummy gate material;

(d) forming a layer of dielectric adjacent said dummy gates;

(e) removing said dummy gates;

(f) depositing gate material on said dielectric and

(g) patterning a second layer of photoresist on a second antireflective layer on said gate material to define gates;

(f) using said patterned photoresist without linewidth reduction to form gates.

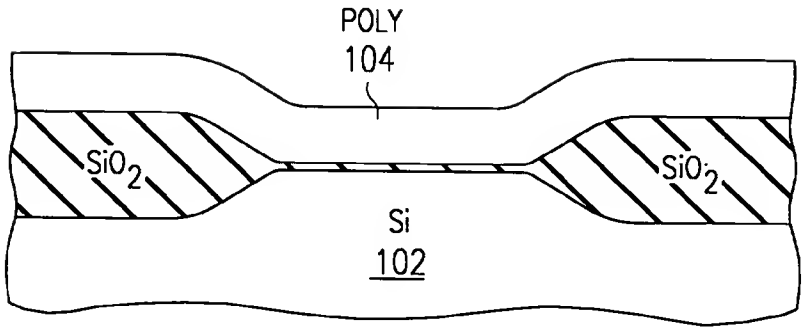


FIG. 1a

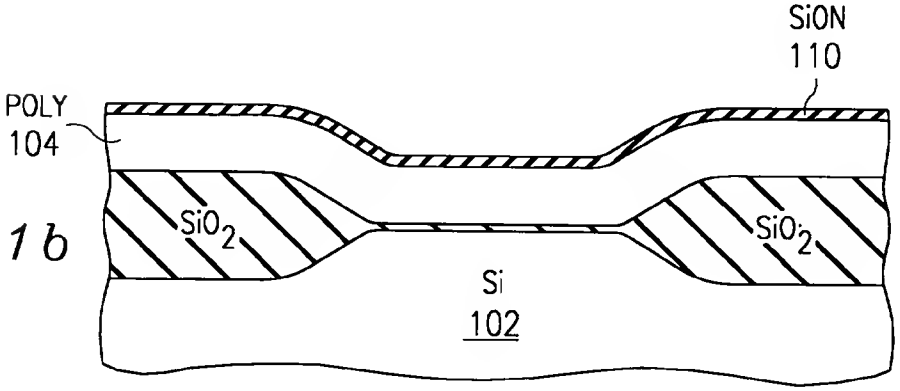


FIG. 1b

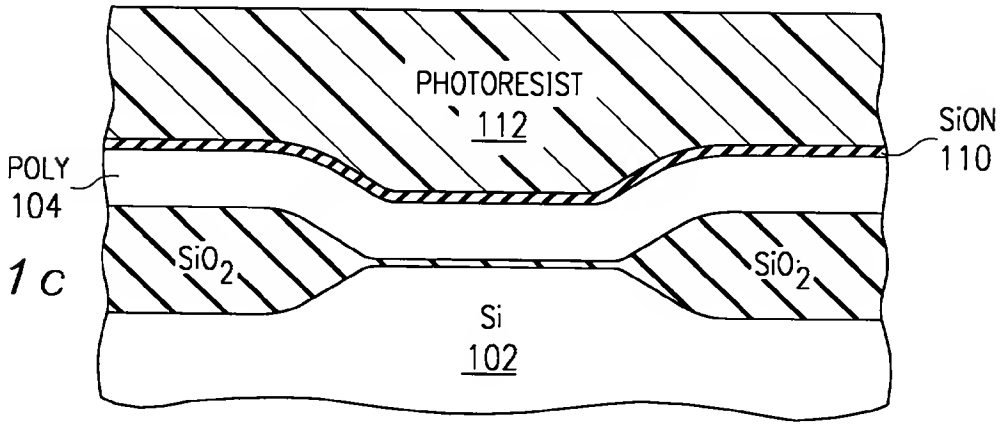


FIG. 1c

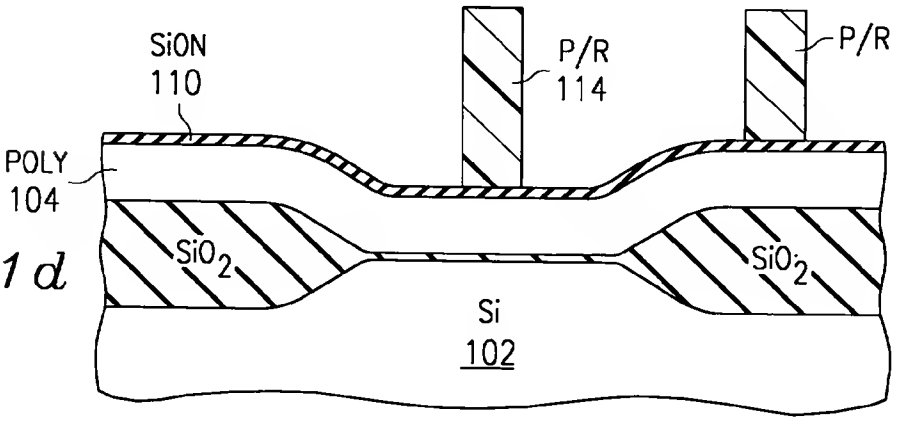


FIG. 1d

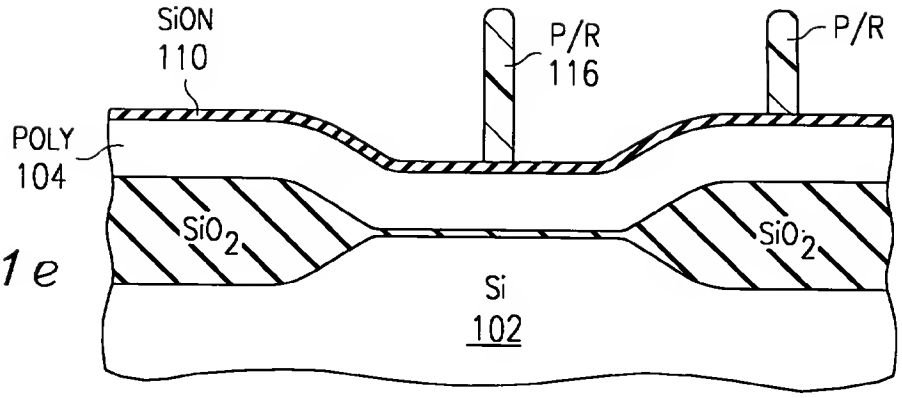


FIG. 1e

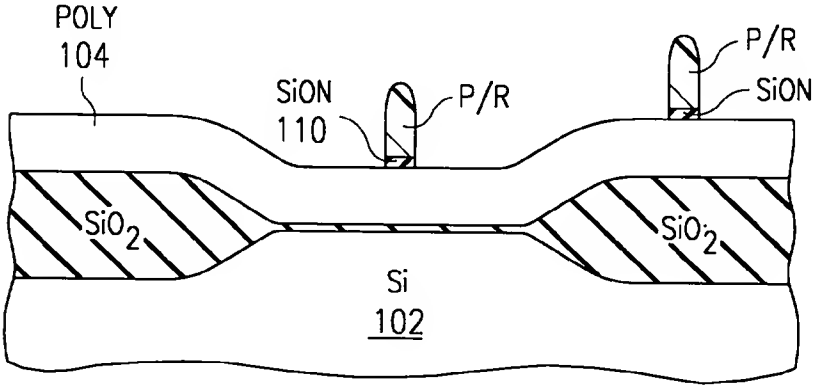


FIG. 1f

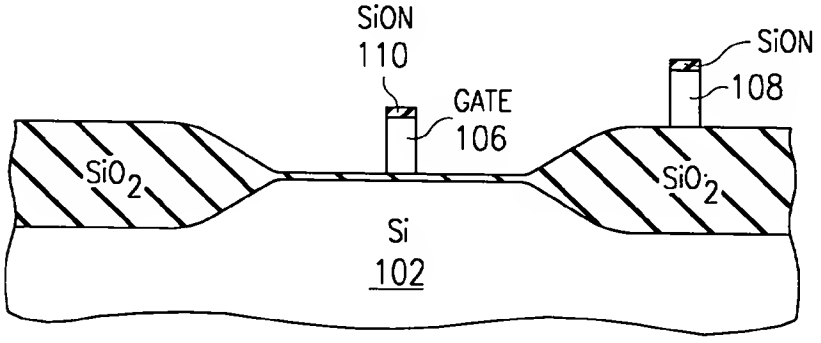


FIG. 1g

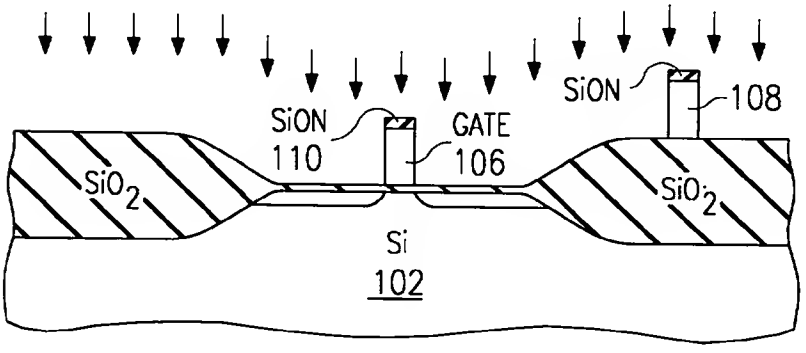


FIG. 1h

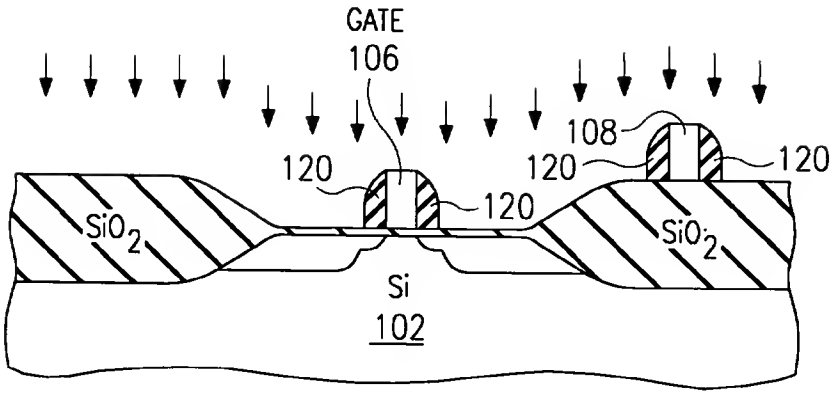


FIG. 1i

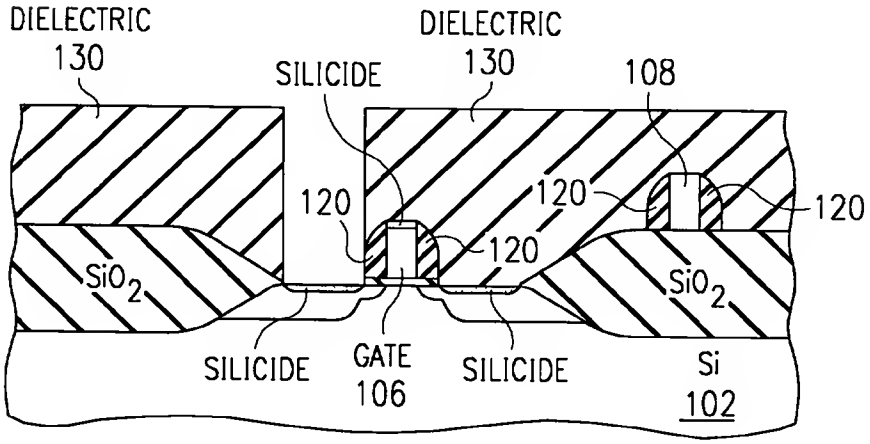


FIG. 1j

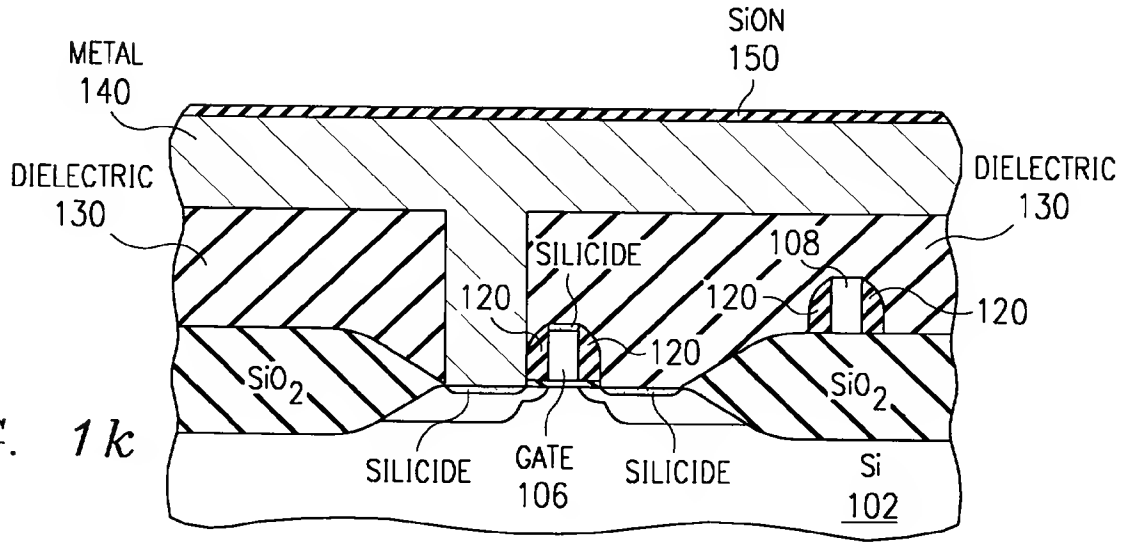


FIG. 1k

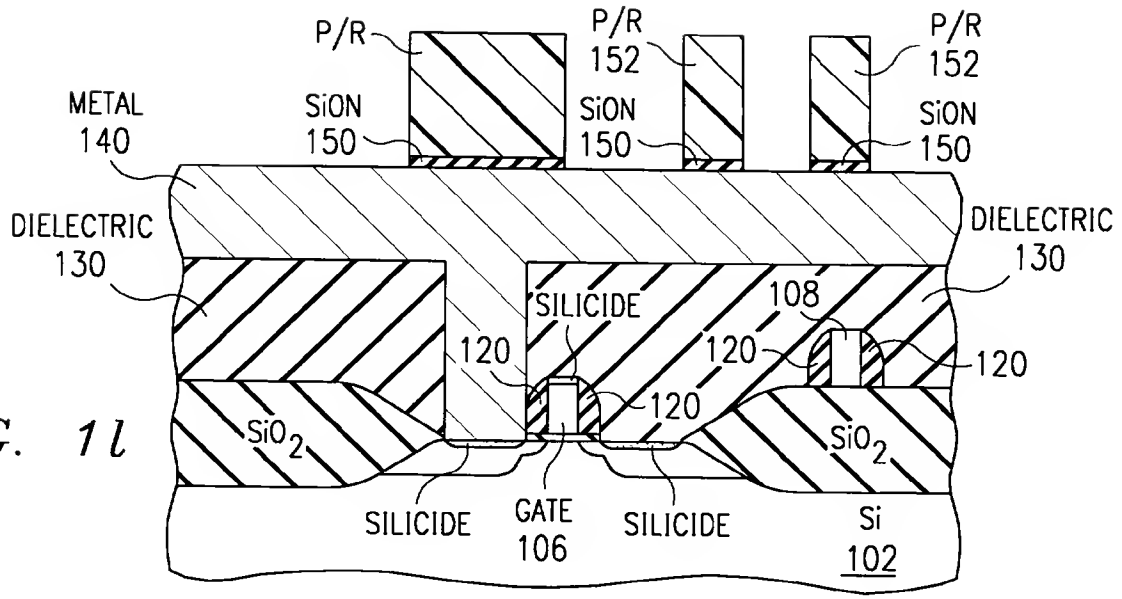


FIG. 1l

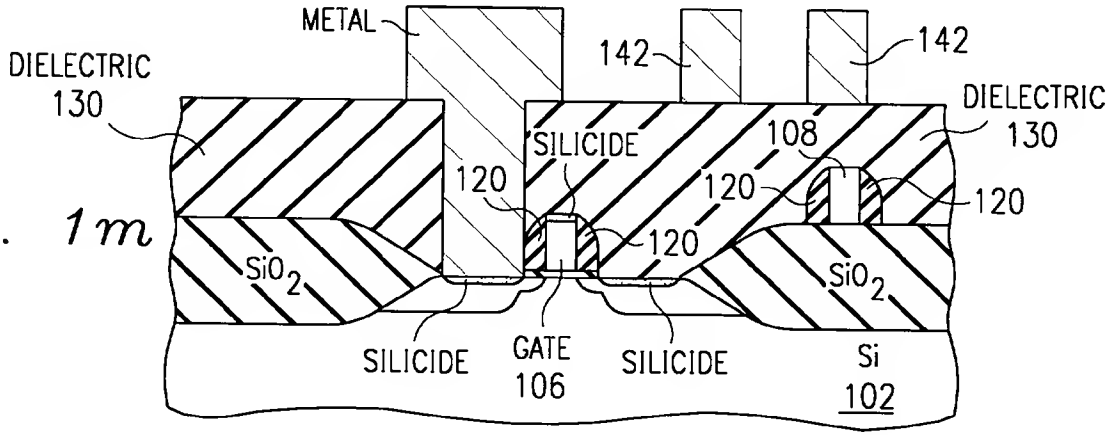


FIG. 1m

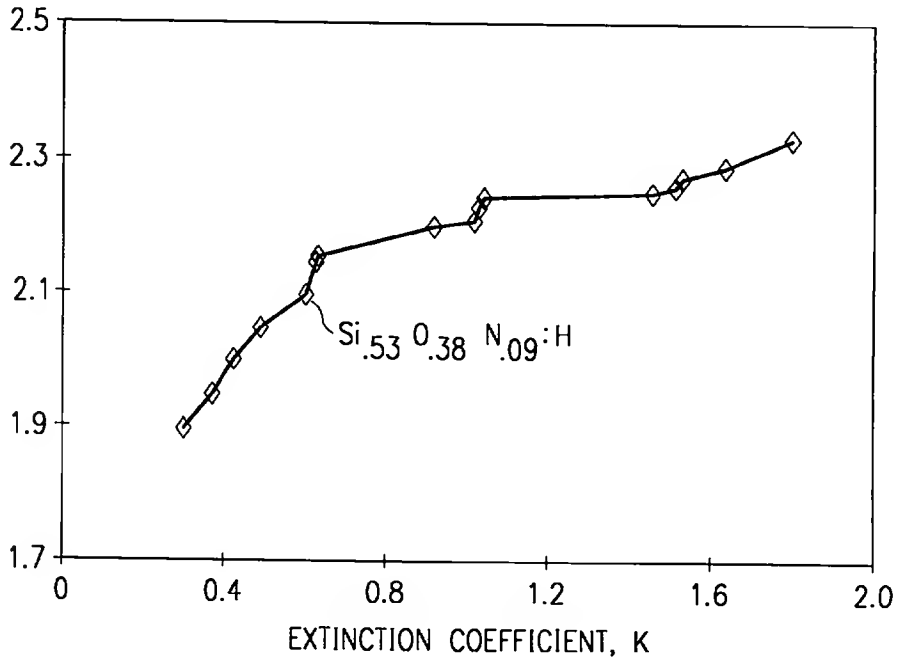


FIG. 2

FIG. 3

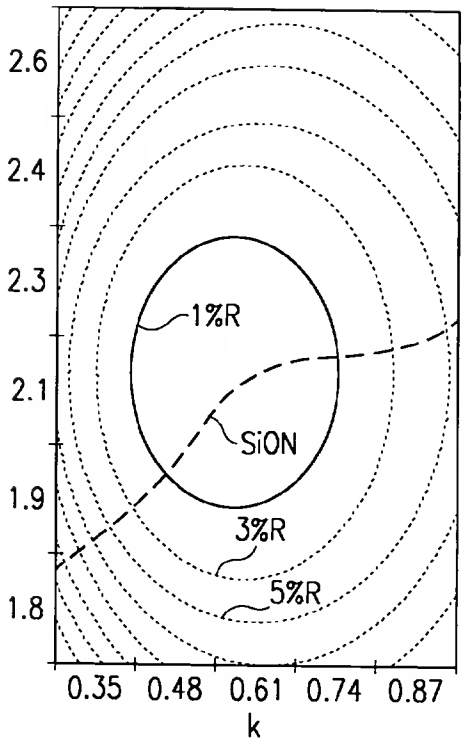


FIG. 4

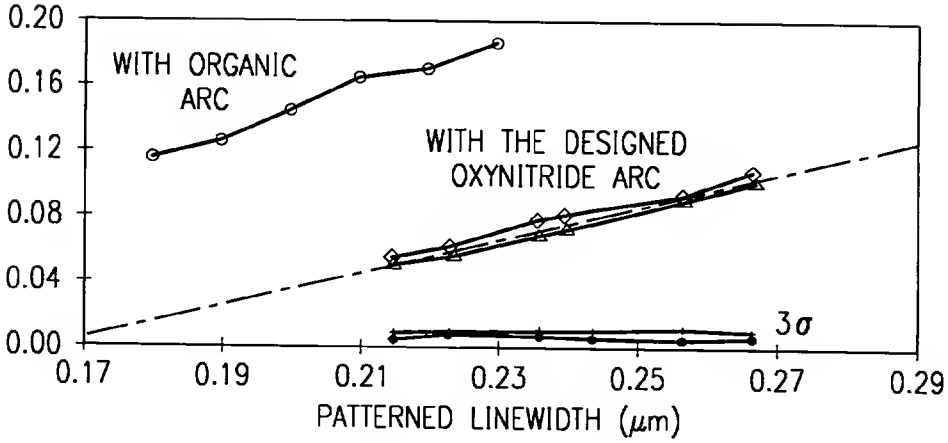
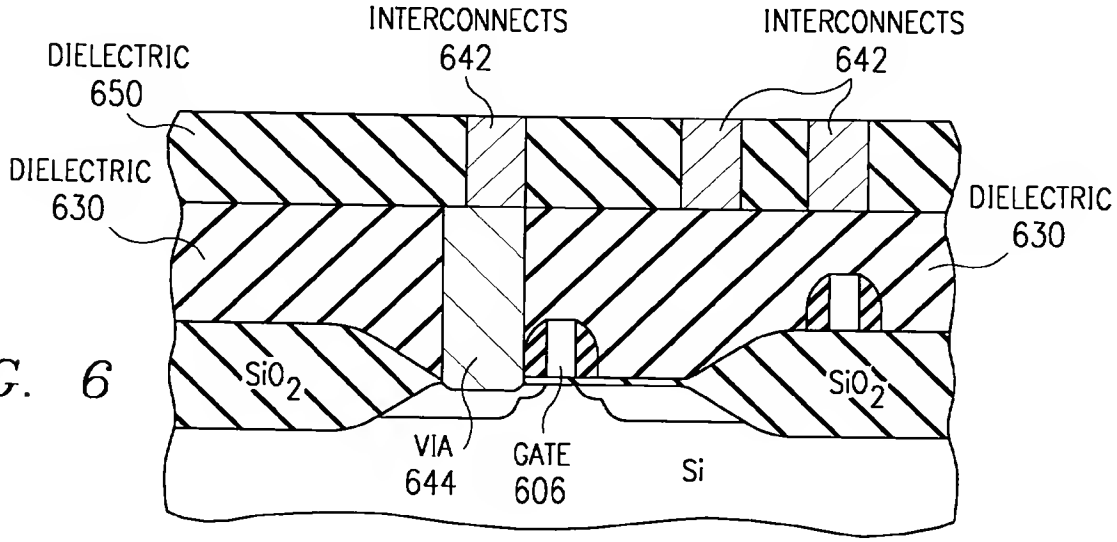


FIG. 6



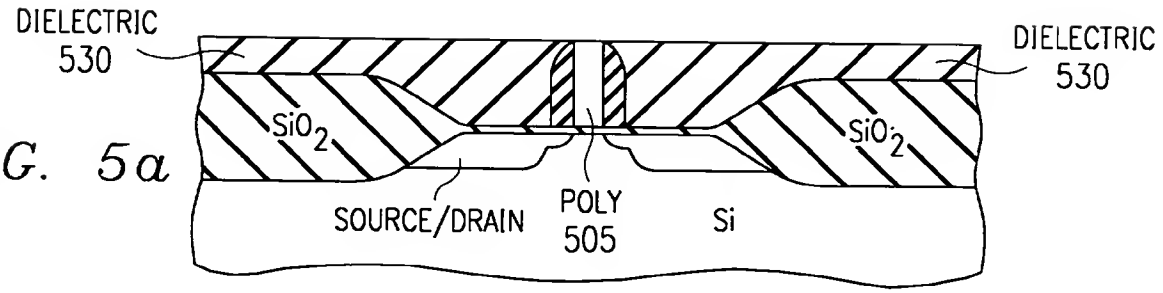


FIG. 5a

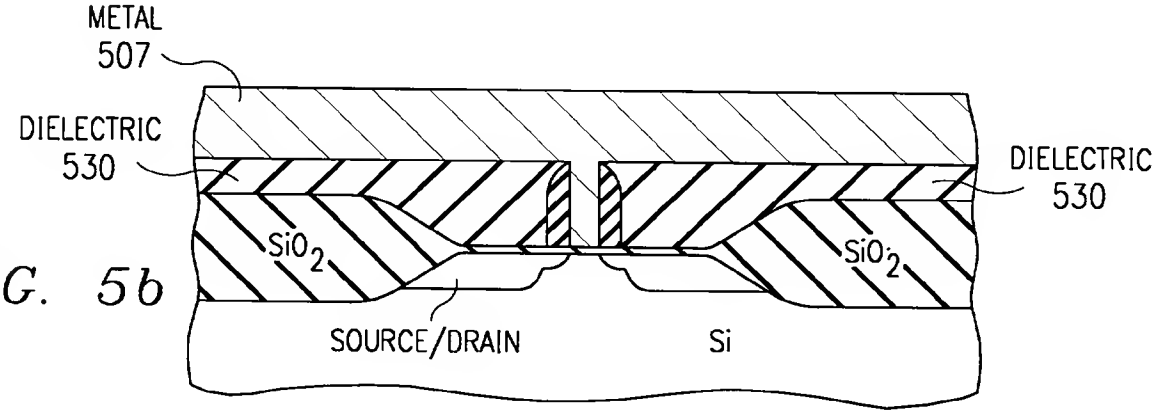


FIG. 5b

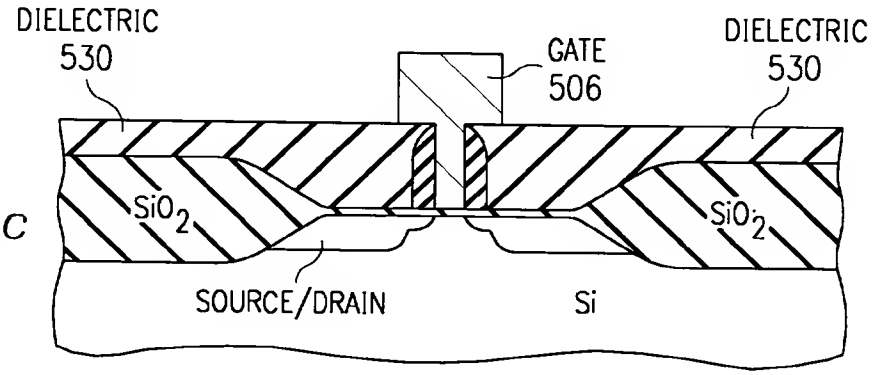


FIG. 5c

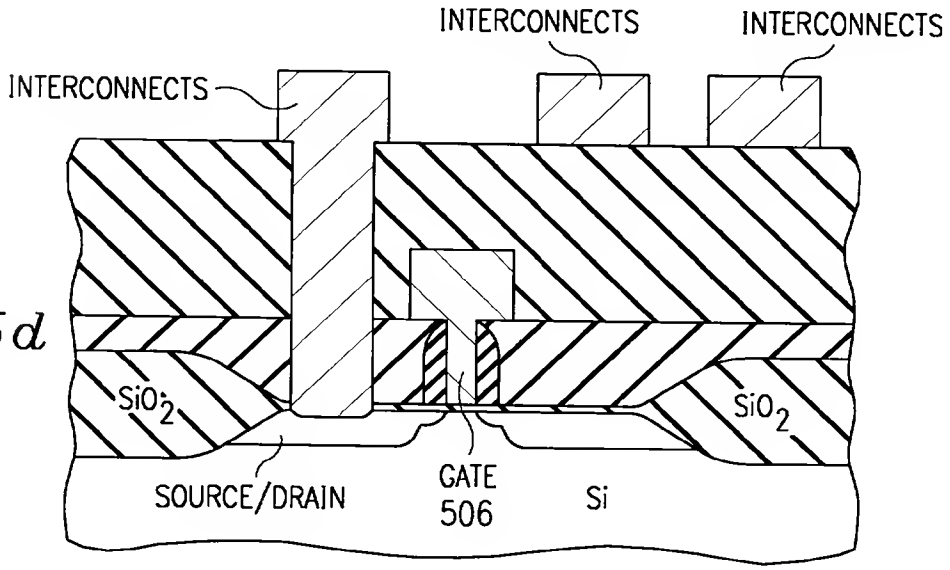


FIG. 5d

Docket No. TI-25277

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, and I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Antireflective Structure and Method**, which:

(a) __X__ is attached hereto.

(b) _____ was filed on **06/05/98** as Serial No. .

(c) _____ was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____ (if any).

I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment specifically referred to in the oath or declaration;

No application for patent or inventor's certificate on this invention has been filed by me or by my legal representatives or assigns in any country foreign to the United States of America;

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations Section 1.56(a);

I hereby claim that benefit under Title 35, United States Code Section 120 of any United States applications listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial No. 60/049,006, filed on 06/09/97.

As a named inventor, I hereby appoint the following attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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Richard L. Donaldson, Reg. No. 25,673;
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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code, and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

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Inventor's signature: _____ Date: _____

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Inventor's signature: _____ Date: _____